Thickness-dependent mobility in tetracene thin-film field-effect-transistors

Jun Shi, De-Tong Jiang, John R. Dutcher, and Xiao-Rong Qin

Citation: Journal of Vacuum Science & Technology B 33, 050604 (2015); doi: 10.1116/1.4931034
View online: http://dx.doi.org/10.1116/1.4931034
View Table of Contents: http://scitation.aip.org/content/avs/journal/jvstb/33/5?ver=pdfcov
Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

Articles you may be interested in

Study on copper phthalocyanine and perylene-based ambipolar organic light-emitting field-effect transistors produced using neutral beam deposition method

Nonvolatile memory thin film transistors using CdSe/ZnS quantum dot-poly(methyl methacrylate) composite layer formed by a two-step spin coating technique

The influence of gate dielectrics on a high-mobility n-type conjugated polymer in organic thin-film transistors
Appl. Phys. Lett. 100, 033301 (2012); 10.1063/1.3678196

Thickness-dependent in situ studies of trap states in pentacene thin film transistors
Appl. Phys. Lett. 96, 083304 (2010); 10.1063/1.3309685

Controlled enhancement of the electron field-effect mobility of F 16 Cu Pc thin-film transistors by use of functionalized Si O 2 substrates
Appl. Phys. Lett. 87, 183504 (2005); 10.1063/1.2117622
Thickness-dependent mobility in tetracene thin-film field-effect-transistors

Jun Shi, De-Tong Jiang, John R. Dutcher, and Xiao-Rong Qin

Department of Physics and Guelph-Waterloo Physics Institute, University of Guelph, Guelph, Ontario N1G 2W1, Canada

(Received 21 June 2015; accepted 3 September 2015; published 21 September 2015)

The authors report the thickness-dependent mobility of tetracene field-effect transistors with silicon oxide as the gate dielectric. The lowest field-effect mobility starts at ~3 monolayers (ML). The mobility increases with film thickness linearly and saturates at ~0.38 cm²V⁻¹s⁻¹ at the coverage of 8 ML. Surface morphology of tetracene films and possible mechanisms that could account for the dependence of the mobility on thickness are discussed. © 2015 American Vacuum Society. [http://dx.doi.org/10.1116/1.4931034]

I. INTRODUCTION

Organic semiconductors have been of significant interest in recent decades because of their great potential in building electronics for low-cost devices on large area and flexible substrates. Since the demonstration of organic field-effect transistors (OFETs), where a thin film of organic molecules acts as the active layer contributing to the current, the mechanism of charge transport in organic materials has not been well understood.¹–⁵ Different from conventional inorganic transistors (OFETs), OFETs appear as interface devices: the charge transport is film thickness-dependent, and a few molecular layers adjacent to the molecule–substrate interface appear dominating the charge transport process. For instance, for α-hexathienylene⁶,⁷ and dihexylquaterthiophene,⁸ the current has been reported to be mainly confined in the first two layers. Whereas the hole mobilities in the OFETs of pentacene⁹–¹¹ and copper-phthalocyanine¹² have been reported to have a saturation thickness of ~6 monolayers (ML). The origin of such variance in the thickness-dependent transport properties apparently calls for further investigation.

Tetracene (C₁₈H₁₂), a π-conjugated polyacene molecule,¹³ consists of four fused benzene rings, with one ring less than the most studied pentacene.⁹,¹⁴,¹⁵ Though the intrinsic mobilities in their single-crystal OFETs are similar,¹⁶ the mobility values for tetracene films are an order of magnitude lower than pentacene films.¹⁷–²⁰ A plausible explanation for this contrast is related to the film structures: While high-quality layered film structures can be readily prepared in pentacene growth on most substrates, tetracene films tend to have three-dimensional island growth with granular structures.¹⁸–²⁹ Our recent work shows that layered film morphology in tetracene growth is achievable on both hydrogen-terminated silicon and silicon oxide surfaces under optimized growth conditions.³⁰–³² However, the electrical characteristics of OFETs made from these layered tetracene films, and the thickness-dependent behaviors have not been explored. In this work, we have fabricated OFETs from layered tetracene films on silicon oxide and investigated the field-effect mobility with different film thickness.

II. EXPERIMENT

To prepare the substrate, the native oxide on a heavily doped Si(001) (~0.01 Ω cm) wafer was removed with hydrofluoric acid after thoroughly cleaned in a hot piranha solution (98% H₂SO₄:30% H₂O₂ ≈ 4:1). A 300 nm-thick silicon oxide layer was then grown by a dry-oxidation method at a temperature of 1050 °C under 1 atm pressure.³³ The thickness of oxide layer was determined with ellipsometry measurements using a Multiskop (Optrel GBR). Tetracene (98%, Sigma-Aldrich) thin film of various thicknesses were grown in an ultrahigh vacuum (base pressure <3×10⁻⁹Torr) onto the as-grown oxide surfaces without any further treatment. An optimized deposition rate at 4 nm/min was used to realize a tetracene layered film morphology.³¹ The deposition rate was monitored by a quartz crystal microbalance. All the film growth was done with the substrate at room temperature. Detailed substrate preparation and film deposition procedures have been reported elsewhere.³⁰–³²

After tetracene deposition, the sample was taken out of the growth chamber immediately (within 5 min) to avoid potential degradation of organic thin film due to the material desorption in ultrahigh vacuum environment.³⁴–³⁶ Then, 15 nm-thick drain (D) and source (S) gold electrodes were thermally evaporated in another vacuum chamber (2 × 10⁻⁵Torr) through a shadow mask to define transistors with 80 µm in channel length and 500 µm or 1000 µm in channel width. A fast gold deposition rate of 30 nm/min was used to avoid gold penetration into organic films, producing low contact resistance between the organic films and gold electrodes.³⁷ Typically, our tetracene film samples stayed in the vacuum chamber for about 1–2 h to complete the gold evaporation. To form the gate (G) electrode, the backside oxide-layer of the silicon substrate was removed by concentrated 49% hydrofluoric acid and gallium/indium paste was then painted over for electrical contact. The electrical characteristics of the transistors were measured manually under ambient condition, with a circuit shown in Fig. 1(a). We used a dual-channel DC power supply (ANATEK) to provide constant voltage inputs for the circuit, and the biases for the drain (V DS) and the gate (V G) electrodes were controlled through adjustable resistors. A current preamplifier (ITHACO 1211) was used to convert the drain current (I DS) to a voltage signal (V A), and to virtually ground S electrode.

*Electronic mail: xqin@uoguelph.ca
film growth problems induced by the presence of metal electrodes can also be avoided (e.g., film discontinuities near metal electrodes),\textsuperscript{5,34} which usually occurs for a bottom-contact FET fabrication scheme.

III. RESULTS AND DISCUSSION

Figure 1(b) shows the typical output characteristics (drain–source current $I_{DS}$ versus drain–source voltage $V_{DS}$ at different gate voltage $V_{G}$) of a tetracene thin-film FET operated in the hole-accumulation (p-type) mode. As shown in Fig. 1, the drain current increases linearly with low drain voltage $|V_{DS}|$ (i.e., $V_{DS} > -10$ V), so-called “linear-regime,” and saturates at high $|V_{DS}|$ (i.e., $V_{DS} < -10$ V), so-called “saturation-regime.” In the linear-regime, the drain current with respect to drain voltage can be modeled by the following expression:\textsuperscript{5}

$$I_{DS} = \frac{W}{L} \frac{e}{t} \mu \left(V_{G} - V_{T} - \frac{V_{DS}}{2}\right)^{2},$$

(1)

where $W$ is the channel width and $L$ the channel length; $e$ and $t$ are the dielectric constant and thickness of the SiO$_2$ layer, respectively; $V_T$ is the threshold gate voltage [activation potential for the conductive channel formation in a FET (Ref. 38)]; and $\mu$ is the field effect mobility of the transistor. By taking a derivative of $I_{DS}$ with respect to $V_{G}$ under a constant $V_{DS}$ using Eq. (1), the transconductance $g$ can be written as a function of the mobility $\mu$,\textsuperscript{5}

$$g = \frac{\partial I_{DS}}{\partial V_{G}} \bigg|_{V_{DS}} = \frac{W}{L} \frac{e}{t} \mu V_{DS}.$$  

(2)

Therefore, by plotting $I_{DS}$ versus $V_{G}$ at a constant low $|V_{DS}|$ [e.g., $V_{DS} = -5$ V in Fig. 1(c)] and taking the slope in the linear part as $g$, we deduce the mobility $\mu$ of the transistor. In this study, only the hole mobility deduced in the linear-regime (i.e., the drain current increases linearly with low drain voltage) are reported because it ensures that we do not overestimate the value of the actual mobility.\textsuperscript{5,39–42}

Figure 2 shows the transfer characteristics for samples of different tetracene thickness. The linear part of a curve usually emerges after $-30$ V. Fitting data for each curve to Eq. (2) yields the linear-regime mobility. Figure 3 illustrates the mobility $\mu$ deduced in the linear-regime ($V_{DS} = -5$ V) as a function of the film thickness $d$. Each data point in Fig. 3 represents the average value of at least three individual tetracene FETs. As shown in Fig. 3, the mobility increases with film thickness dramatically by nearly 2 orders of magnitude, from $0.0017 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at 3 ML to $\sim 0.38 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at $\geq 8$ ML. The highest mobility of tetracene FETs we tested so far is $\sim 0.58 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ (Fig. 3). The trend in the data points is well represented by a fit (solid line in Fig. 3) using the empirical equation proposed by Dinelli et al.,\textsuperscript{7} which has been characteristic for many organic semiconductors,\textsuperscript{7,8,12}

$$\mu = \mu_{sat}\left(1 - \exp[-(d/d_0)^\gamma]\right),$$

(3)

where $\mu_{sat}$ is the saturated mobility, $d_0$ is the saturation thickness, and $\gamma$ is the fitting exponent.

Three digital voltmeters were used to measure $V_{DS}$, $V_{G}$, and $V_A$, respectively. The typical measurement speed was a few seconds per voltage step of 1 V. Right after being prepared, the tetracene films, either as-grown or after the gold evaporation, were imaged with an atomic force microscopy (AFM) (Digital Instruments DimensionTM 3100) using tapping mode. Silicon cantilevers (model OMCL-AC160TS, $k = 26$ N/m, $f_0 = 300$ kHz, Olympus) were used for the AFM imaging. The typical scan rate is $\sim 1$ Hz per scan line.

In order to maintain the integrity of the SiO$_2$ substrate surface to avoid any possible contamination at the tetracene–substrate interface, only aforementioned top-contact FET fabrication scheme has been employed as shown in Fig. 1(a). With this top-contact scheme, some other

![Fig. 1. (a) Circuit diagram for measuring electrical characteristics of the tetracene top-contact FETs. Typical electrical characteristics of a tetracene FET (21.8 ML in film thickness): (b) drain current $I_{DS}$ vs drain voltage $V_{DS}$ at various gate voltage; (c) drain current $I_{DS}$ vs gate voltage $V_{G}$ at a constant drain voltage $V_{DS} = -5$ V in the linear-regime.](image-url)
Using the least square fitting algorithm, we obtain the following numerical values: the saturated mobility \( \mu_{\text{sat}} = 0.38 \pm 0.04 \text{cm}^2\text{V}^{-1}\text{s}^{-1} \), the saturation thickness \( d_0 = 8.0 \pm 0.5 \) ML, and the fitting exponent \( \alpha = 6.0 \pm 2.4 \). For two different width/length ratios (i.e., \( W/L = 500/80 \) and \( W/L = 1000/80 \)) in the tetracene FETs prepared following the same process, we have obtained the same consistent saturated mobility without noticeable difference. The saturated mobility we obtained is so far the highest, to our best knowledge, for tetracene thin film FETs reported in literature 17–26.

Compared with the intrinsic mobility (2.4 cm\(^2\)V\(^{-1}\)s\(^{-1}\)) obtained in tetracene single-crystal FETs, 16 the mobility values extracted here for tetracene film FETs are effective ones which are convoluted with several practical factors. Vacuum-deposited films are polycrystalline, with a significant number of small crystallites, grains, and grain boundaries. Also, carrier injection process may involve contact problems. 5,16 Higher density of grain boundaries near the Au electrode than in the channel area has been found in the bottom-contact FETs, causing significant charge trapping near the electrode, limiting the charge transport hence the mobility. 5 However, this is not the case for the top-contact FETs, and most high-performance pentacene film FETs reported in the literature have the top-contact configuration. 5 The linear-regime mobility can be affected by contact problems, without contact resistance characterization, the mobility extracted from Eq. (2) tends to be underestimated. 5,39

Other carrier trapping factors, such as pronounced hysteresis 39 (possibly due to bias-stress induced defects) and water formation 40 at the substrate–molecule interface, can also effectively lower the mobility value in measurements. Our tetracene film FETs has the top-contact configuration, and the mobility values are extracted exclusively from the linear-regime under forward measurement direction; hence, these mobility values are established in a conservative manner. With all the top-contact FETs consistently prepared and measured under the same experimental conditions, and with the results obtained (Fig. 3) similar to other organic semiconductors, 7,9,12 we attribute the observed relative change of mobility at different thickness to the structural properties of the tetracene film.

We have examined the surface morphology of tetracene thin films at various thicknesses, before and after gold deposition. Figure 4(a) shows an as-grown film (3 ML) which has good connectivity with some exposure of second layer (see the AB line profile). Our previous AFM work 30 shows that a new growth mode starts above the third molecular layer, and with near edge x-ray absorption fine structure, we also find a structure phase transition occurring at 3 ML. 32 These are consistent with the 3D islands appeared in the image. But after the gold deposition, the tetracene film is dramatically deteriorated [Fig. 4(b)] with significant exposure of the substrate. Further increasing the coverage to 4.4 ML [Fig. 4(c)], the film connectivity appears less influenced by the gold deposition procedure, as less area exposure of the substrate is found in Fig. 4(d). We further increase the film coverage up to 6.1, 8.8, and 17.5 ML, respectively, and all these films are well-connected as shown in Fig. 5. No visible changes in the film connectivity were found between an as-grown film and the film after gold deposition.

We attribute two factors being responsible to influence the connectivity for the low-coverage films (<6 ML, i.e., before the completion of the third layer over the entire surface): (1) the metastable nature of the film; and (2) vacuum desorption during gold contacts formation. Our earlier work shows that the stability of the tetracene films on SiO\(_2\) is...
That is, mass transport occurs at film step edges, from the lower layer to the higher layer; and always occurs in areas where thickness is thinner than 3 molecular layers. The mass transport happens in air, as well as in vacuum. The low-coverage films are therefore metastable, and susceptible to change into poorly connected films. As shown in Figs. 4(b) and 4(d): line profiles CD and GH indicate that the island edges are at least 3 molecular layers high, without any traces of lower height step edges, consistent with the metastable-film picture. On the other hand, for the specific gold evaporation system used in this work, the film has to be kept inside vacuum for \( \sim 1–2 \) h. We find that without the gold deposition, only keeping the low-coverage films in the vacuum for 2 h, the films also deteriorate to a similar degree as those shown in Figs. 4(b) and 4(d). Therefore, vacuum desorption could be a major extrinsic factor for the metastable film to decay.

Following the coverage-dependent film-stability results, we may also understand the cause of the higher stability for high-coverage films (>6 ML, as shown in Fig. 5): the surface is completely covered by stable islands (i.e., local thickness \( \geq 3 \) molecular layers), hence significantly reducing the film decay. It turns out that \( \sim 6 \) ML [Fig. 5(a)] appears to be the critical nominal thickness for the completion of the 3rd molecular layer everywhere on the as-grown film, leading to a stable film without much film deterioration in the further processing.

The thickness-dependent mobility data in Fig. 3 reveal three facts. First, the lowest measurable mobility starts at \( \sim 3 \) ML, suggesting that the minimum effective conducting-area is \( \sim 63\% \) [as shown by the film covering area in Fig. 4(b)], the threshold for establishing significant electrical conducting pathways in the channel of the FET. Compared with the percolation threshold 67\% (i.e., the surface coverage when islands come into contact for a continuous two-dimensional system\(^{43}\)), the few percentage difference could be due to the fact that our films with layered architecture are not a two-dimensional system, and thus involve complicated percolation geometry.\(^{43,44}\)

Second, the growth mode transition is not a major limiting factor to \( \mu \). We know that the film roughening transition from quasi-layer-by-layer (2D) growth to mound-type 3D island growth starts at \(<3 \) ML,\(^{30,32}\) which is well below the mobility saturation thickness \( (d_0 \sim 8 \) ML).

Third, saturation thickness \( d_0 \) for our tetracene FETs is \( \sim 8 \) ML, about 1–2 ML thicker than that reported for pentacene case,\(^{5,11}\) despite that the two molecules resemble a similar crystalline molecular structure\(^{12}\) and film morphology.\(^{30,31}\) The major reason for the mobility increase from 6 to 8 ML for tetracene films cannot be explained with the film

![Fig. 4. AFM images (10 \times 10 \,\mu m) of tetracene films: (a) 3 ML as grown, and (b) the same film after gold deposition; (c) 4.4 ML as grown, and (d) the same film after gold deposition. Substrate surface coverage percentages for (b) and (d) are \( \sim 63\% \) and \( \sim 88\% \). The root-mean-square (RMS) values of the images are (a) 2.10 nm, (b) 4.05 nm, (c) 3.01 nm, and (d) 3.79 nm.](image)

![Fig. 5. AFM images (10 \times 10 \,\mu m) of tetracene films with coverage of (a) 6.1 ML, (b) 8.8 ML, and (c) 17.5 ML after the process of gold deposition. The corresponding RMS values are (a) 3.64 nm, (b) 4.49 nm, and (c) 6.37 nm. The grain size appears increasing with coverage, from typical \( \sim 1 \,\mu m \) in (a) to \( \sim 1.5–2 \,\mu m \) in (c).](image)
connectivity. Figure 5 shows that the films, from 6 to 17.5 ML, are all well connected.

We hypothesize that the high density of crystalline domains (or density of domain boundaries) and stack anisotropy may effectively influence the percolation path and the saturation coverage. Recently, in situ measurements of drain-source current versus the saturation coverage in pentacene FETs show that the results depend on growth mode and deposition rate. The channel depth where the current primarily resides and the spatial charge carrier distribution along the depth depend on the molecule stacking morphology and are thus modulated by the growth mode. These in situ measurements suggest that spatial distribution of charge carriers may provide new insight of the charge transport process. In our tetracene film growth, the deposition rate required is rather high (over three times higher than the pentacene case). Using grazing-incidence x-ray diffraction and AFM, we reported that the single-crystal domain size and its anisotropy are coverage-dependent; and that they sensitively depend on the interface structure such as substrate steps (but the top surface islands, which can be orders of magnitude bigger, remain unaffected). Domain boundaries are structure defects which may act as carrier traps to influence carrier transport. Presumably, for our tetracene films, additional 2 ML beyond the 6 ML (for a completely connected film) is helpful in providing necessary percolation paths to bridge across the layered architecture and the domain boundaries, hence to increase the saturated mobility at 8 ML. Further studies on the charge carrier distribution across layers, in correlation to the domains stacking and anisotropy, would be helpful to better understand the insight.

IV. SUMMARY AND CONCLUSIONS

We have fabricated top-contact tetracene FETs on SiO2 substrate and characterized the field-effect mobility of the FETs as a function of the tetracene film thickness. We have obtained the saturation mobility of $\mu_{sat} = 0.38 \pm 0.04 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$. The lowest measurable carrier mobility starts at ~3 ML of the tetracene film, then the mobility increases linearly with the thickness, and saturates at a thickness of 8 ML. For two different channel width/length ratios (i.e., W/L = 500/80 and W/L = 1000/80) in the tetracene FETs, the same consistent saturated mobility is obtained. The dependence of the mobility on the film thickness is discussed in the context of the film surface morphology and related film connectivity. We attribute that the film stability and connectivity are primarily responsible for the increase of mobility with the film thickness up to 6 ML. Further enhancement of the mobility with the film thickness (between 6 and 8 ML) could be related to the crystalline domain density (or domain boundary density), which is thickness-dependent as revealed by our previous surface x-ray diffraction and AFM studies.

ACKNOWLEDGMENTS

This work was supported in part by Natural Science and Engineering Research Council of Canada (NSERC), and Canada Foundation for Innovation (CFI) and Ontario Innovation Trust (OIT).

34. J. Shi and X. R. Qin (unpublished results): (a) The gold and tetracene-film joint has been imaged with AFM, no visible disconnectivity was observed; (b) AFM of the tetracene films after being kept in ultra-high vacuum for few hours, shows a significant film decay.